

REMARKS

Applicants appreciate the detailed examination evidenced by the Office Action mailed June 23, 2006 (hereinafter "Office Action"). With respect to filing of a translation of the priority application, Applicants submit that the Office Action misconstrues the requirements of 35 U.S.C. § 119 and asserts a requirement for a translation in what appears to be an inappropriate context, as no intervening reference has been cited in rejecting the claims, and interference does not appear to be under consideration given the nature of the current substantive rejections.

Applicants have amended Claims 2-10 and 12-14 to replace "A" with --The-- as requested on page 2 of the Office Action. Applicants have also amended Claim 6 to correct the typographical error noted on page 3 of the Office Action, have amended Claim 7 to correct the antecedent basis error at line 4 noted on page 3 of the Office Action, have amended Claim 8 to correct the antecedent basis error at line 7 noted on page 3 of the Office Action and have amended Claim 9 to correct a typographical error at line 4 and the antecedent basis error at line 5 noted on page 3 of the Office Action. Applicants respectfully traverse others of the alleged informalities and indefiniteness rejections on pages 2-5, as the Office Action, in raising these objections and rejections, adopts syntactical rules that are not supported by the cited legal standards. Applicants also traverse the rejections of Claims 1-14 based on U.S. Patent No. 5,293,386 to Muhmenthaler et al. (hereinafter "Muhmenthaler") for at least the reason that Muhmenthaler does not provide several of the teachings alleged in the Office Action.

Priority

The Office Action incorrectly states that 35 U.S.C. §119(b) requires filing of "a certified copy of the English language translation." 35 U.S.C. § 119(b) states:

(3) The Director may require a certified copy of the original foreign application, specification, and drawings upon which it is based, a translation if not in the English language, and such other information as the Director considers necessary. Any such certification shall be made by the foreign intellectual property authority in which the foreign application was filed and show the date of the application and of the filing of the specification and other papers.

M.P.E.P. § 201.2(b) further states:

The papers required are the claim for priority and the certified copy of the foreign application.

...

The certified copy that must be filed is a copy of the original foreign application with a certification by the patent office of the foreign country in which it was filed.

Certified copies ordinarily consist of a copy of the specification and drawings of the applications as filed with a certificate of the foreign patent office giving certain information.

Applicants filed a certified copy of the original foreign application meeting these requirements on August 26, 2005.

Applicants note that a translation may be required under certain circumstances, but that these circumstances do not appear to be applicable to the present application. In particular, M.P.E.P. § 201.15 states:

The only times during *ex parte* prosecution that the examiner considers the merits of an applicant's claim of priority is when a reference is found with an effective date between the date of the foreign filing and the date of filing in the United States and when an interference situation is under consideration. If at the time of making an action the examiner has found such an intervening reference, he or she simply rejects whatever claims may be considered unpatentable thereover, without paying any attention to the priority date (assuming the papers have not yet been filed). The applicant in his or her reply may argue the rejection if it is of such a nature that it can be argued, or present the foreign papers for the purpose of overcoming the date of the reference. If the applicant argues the reference, the examiner, in the next action in the application, may specifically require the foreign papers to be filed in addition to repeating the rejection if it is still considered applicable, or he or she may merely continue the rejection.

The Office Action does not cite any such intervening references, and there appears to be no consideration of an interference, given that several of the claims stand rejected as allegedly anticipated by a patent that issued well before the effective filing date of the present application. Accordingly, Applicants submit that the requirement for a certified translation of the priority application is improper, unnecessary to address the rejections and would require Applicants to incur unnecessary expense. Applicants, therefore request the

requirement be withdrawn. Should this requirement be maintained, Applicants respectfully request clarification of the grounds for the requirement.

The claim objections

Applicants have amended claims 2-10 and 12-14 to replace "A" with "The" as requested. Applicants have also amended Claims 6 and 8 to correct the typographical errors noted in the Office Action. Applicants have also amended Claim 3 to include the suggested change to "enable the subsets," and has similarly amended Claim 2.

Applicants respectfully traverse the other claim objections. As an initial matter, in these objections, the Office Action adopts syntactical rules that are not supported by any particular legal standard and suggests claim changes that actually may introduce errors and change the meaning of the claims. With respect to Claim 3, the suggested change to "the first externally-applied" could potentially create an antecedent basis error. The phrase as currently written introduces a new claim element, *i.e.*, "first externally-applied control signals," and, thus, is correct.

Regarding Claim 8, the Office Actions suggests change to "a first of the plurality of group control signals . . . because the limitation follows Claim 3." Office Action, p. 3. Applicants first note that "a plurality of group control signals" is introduced in Claim 4, not Claim 3. Furthermore, Applicants submit that the proposed change is unnecessary.

Respectfully, the Office Action appears to be objecting to some of the claim language simply because of the absence of explicit linkages between phrases that use related terms, without consideration of whether the phrasing is actually incorrect, ambiguous or otherwise deficient. For example, the suggested amendment of Claim 8 to recite "a first of the plurality of group control signals" is unnecessary. Claim 4 recites "a data output controller circuit configured to receive a plurality of group control signals", and Claim 8 cites "a voltage comparison circuit which, in response to a first state of a first write inhibit buffer enable signal, compares a write inhibit signal to a reference voltage and outputs a first group control signal responsive to the comparison." It is entirely appropriate to recite "a first group control signal," as this is the first time this element is introduced, and there is nothing inconsistent about this phrasing vis a vis Claim 4.

In light of the foregoing, Applicants request that these objections to Claims 3 and 8 be withdrawn.

The §112 rejections

The Office Action asserts that "'the write inhibit signal buffer control circuit' in line 4" of Claim 7 lacks antecedent basis. Office Action, p. 3. Applicants note that this error actually appears to be in line 2, and have amended Claim 7 to correct the error. Claim 9 has been amended to correct the antecedent basis error in the phrase "the external clock."

The Office Action asserts that Claim 8 is indefinite due to the use of the phrase "a first write inhibit buffer enable signal," as "the examiner is not sure if the limitation refers to claim 7 or to a new instantiation of a signal." Office Action, p. 3. Applicants submit that these recitations are not indefinite, as the Office Action has created a false dichotomy, *i.e.*, it is not a question of whether the recited element is a previously recited element *or* a "new instantiation." "A first write inhibit buffer enable signal" *could* refer to the "write inhibit buffer enable signal" recited in Claim 7, but is not *required* to be as such. In more general terms, in the portion of Claim 7 in question, a new element is recited with an indefinite article "a", *i.e.*, "a first write inhibit buffer enable signal."

Respectfully, the Office Action appears to be creating a requirement for linkages among claim terms that are not required to provide definiteness, and further appears to be confusing claim breadth with indefiniteness. Referring to M.P.E.P. § 2173.04:

Breadth of a claim is not to be equated with indefiniteness. *In re Miller*, 441 F.2d 689, 169 USPQ 597 (CCPA 1971). If the scope of the subject matter embraced by the claims is clear, and if applicants have not otherwise indicated that they intend the invention to be of a scope different from that defined in the claims, then the claims comply with 35 U.S.C. 112, second paragraph. Undue breadth of the claim may be addressed under different statutory provisions, depending on the reasons for concluding that the claim is too broad. If the claim is too broad because it does not set forth that which applicants regard as their invention as evidenced by statements outside of the application as filed, a rejection under 35 U.S.C. 112, second paragraph, would be appropriate. If the claim is too broad because it is not supported by the original description or by an enabling disclosure, a rejection under 35 U.S.C. 112, first paragraph, would be appropriate. If the claim is too broad because it reads on the prior art, a rejection under either 35 U.S.C. 102 or 103 would be appropriate.

Similar arguments apply to several others of the § 112 rejections, including the rejections based on the phrase "first group control signal" in Claim 8, the rejection based on the phrase "an output control signal" in Claim 9 and the rejection based on the phrase "data input/output pins" in Claim 12.

The Office Action further states:

... according to the drawings, the applicant invention connects input/output pins that are common to external data lines. But the claim restricts the input/output pins to an external data line, and so the claim is indefinite because it reads different than the drawings and Disclosure state.

Office Action, p. 11. Respectfully, the alleged discrepancy does not exist. Common connections of multiple data pins to an external data line as recited in Claims 12 and 13 are clearly shown, for example, in FIG. 10, and explained in the specification at page 16, lines 3-17. In particular, Claim 12 recites "connecting data input/output pins coupled to first and second data output circuits of respective first and second subsets of the plurality of data output circuits in common to an external data line." An example of such recitations is shown in FIG. 10, where, for example, a pair of pins from groups 330 and 340 is connected in common to a line that is external to the device 300, just as recited in Claim 12. For at least these reasons, Applicants submit that these rejections are erroneous and should be withdrawn.

Independent Claims 1 and 11 are patentable

In rejecting independent Claims 1 and 11 as being anticipated by Muhmenthaler, the Office Action asserts that Fig. 2 of Muhmenthaler discloses "a plurality of data output circuit (FIG. GPIO), respective ones of which are configured to receive data from respective internal data lines (FIG. 2 GPDB) and respective ones of which are coupled to respective data input/output pins (FIG. 101, 102); and a data output control circuit (FIG. 2 CONTROL) operative to selectively enable subsets of the plurality of data output circuits (FIG. 2 GPAD) to drive their respective corresponding data input/output pins." Office Action, p. 5. Applicants respectfully submit that these assertions are erroneous.

Referring to Fig. 2 of Muhmenthaler, the outputs of the respective group input/output units GPIO are connected to respective input/output data busses IODB, and the input/output data busses are connected to a memory array input/output unit MAIO, which is common to

all the group data input/output units GPIO. *See* Muhmenthaler, column 5, lines 19-50.

Outputs of the memory array input/output unit MAIO are connected to external pads PD and internal auxiliary pads PDx, and the MAIO. The internal auxiliary pads PDx, which support a parallel test mode, are accessible only when the device is not packaged. *See* Muhmenthaler, column 4, lines 12-65. There is nothing in Muhmenthaler that discloses or suggests that the group input/output units GPIO are selectively enabled "to drive a load at their respective corresponding data input/output pins coupled to respective data input/output pins" as recited in Claim 11 or in related apparatus recitations of Claim 1 because, among other things, the group data input/output units GPIO do not *drive* the external pads PD and the internal auxiliary pads PDx. Rather, the group data input/output units GPIO drive the input/output data busses IODB. Moreover, the Office Action provides no specific indication of any particular *selective* operation of the group input/output units GPIO, and Applicants submit that such selective operation of the group input/output units GPIO is neither disclosed nor suggested in Muhmenthaler. Accordingly, Applicants submit that Muhmenthaler does not disclose or suggest all of the recitations of Claims 1 and 11 and that, for at least these reasons, Claims 1 and 11 are patentable over Muhmenthaler.

The dependent claims are patentable

Applicants submit that dependent Claims 2-10 and 12-14 are patentable at least by virtue of the patentability of the various ones of independent Claims 1 and 11 from which they depend. Applicants further submit that several of the dependent claims are separately patentable.

For example, Claim 2, which stands rejected as anticipated by Muhmenthaler, recites "wherein the data output control circuit is operative to selectively cause subsets of the plurality of data output circuits to present a high impedance at their respective corresponding data input/output pins." In rejecting Claim 2, the Office Action cites column 17, lines 43-45, which merely indicates the read units RDU2 (see Muhmenthaler, FIG. 11) connected to the internal pads PDx have a high impedance state in a normal operating mode. However, this does not provide selective operation of subsets corresponding to the respective group data input/output units GPIO; rather, the high impedance state is imposed for *all* of the internal pads PDx. Accordingly, Muhmenthaler does not disclose or suggest the recitations of

Claim 2 and, for at least these reasons, Applicants submit that Claim 2 is separately patentable. At least similar reasons support the separate patentability of Claim 13.

Claim 4, which also stands rejected as anticipated by Muhmenthaler, recites:

a data output controller circuit configured to receive a plurality of group control signals and operative to generate respective output control signals responsive to respective ones of the group control signals; and

a plurality of write inhibit signal input buffer circuits; respective ones of which are configured to receive respective ones of a plurality of externally-applied write inhibit signals and operative to generate respective ones of the group control signals therefrom; and

wherein respective subsets of the plurality of data output circuits are configured to receive respective ones of the output control signals and are operative to be enabled and disabled responsive thereto.

In rejecting Claim 4, the Office Action asserts that memory array write units MAWR and memory array read units MARD of Fig. 9 correspond to the recited "write inhibit signal input buffer circuits" that generate the "group control signals" applied to the data output controller circuit (allegedly the circuit CONTROL shown in FIG. 2 of Muhmenthaler). *See* Office Action, p. 6. Applicants submit that this comparison is erroneous. The memory array write units MAWR and memory array read units MARD are part of the memory array input/output unit MAIO (see Muhmenthaler, column 15, lines 11 and 12) and it can be clearly seen in FIG. 2 that no signaling is applied by the memory array input/output unit MAIO to the control circuit CONTROL. Moreover, the memory array write units MAWR and memory array read units MARD simply are not "write inhibit signal input buffer circuits" because *they do not buffer write inhibit signals*; rather, they buffer read and write data between the input/output lines IODB and the output pads PD, PDx. Accordingly, Muhmenthaler does not provide the alleged teachings and, for at least these reasons, Applicants submit that Claim 4 is separately patentable. At least similar reasons support the separate patentability of Claims 5-7 and 14, as these claims include specific recitations relating to operation responsive to write inhibit signals that simply are not disclosed or suggested by Muhmenthaler.

Claim 12, which also stands rejected as anticipated by Muhmenthaler, recites:

... connecting data input/output pins coupled to first and second data output circuits of respective first and second subsets of the plurality of data output circuits in common to an external data line; and

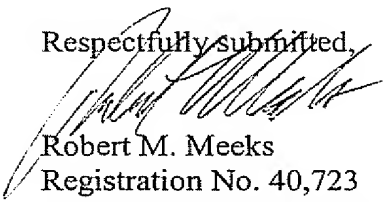
alternately enabling the first and second data output circuits responsive to the control signal to drive the external data line with data from first and second different internal data lines of the memory device.

The Office Action cites Fig. 2 of Muhmenthaler as allegedly disclosing the recited connection to an external data line, but this simply is not shown in FIG. 2 because FIG. 2 does not show any external data line connections to the pads PD, PDx, much less the common external data line connection recited in Claim 12. As no external data line connection is shown, FIG. 2 of Muhmenthaler also clearly does not disclose or suggest "alternately enabling the first and second data output circuits responsive to the control signal to drive the external data line with data from first and second different internal data lines of the memory device." Accordingly, Muhmenthaler does not disclose or suggest the recitation of Claim 12 and, for at least these reasons, Applicant submits that Claim 12 is separately patentable.

Conclusion

As all of the claims are now in condition for allowance, Applicants respectfully request allowance of the claims and passing of the application to issue in due course. Applicants urge the Examiner to contact Applicants' undersigned representative at (919) 854-1400 to resolve any remaining formal issues.

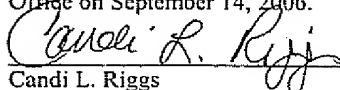
Respectfully submitted,


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